IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	David F. Tobias et al.		
Title:	METHOD AND APPARATUS FOR IMPROVING RESPONSIVENESS OF A POWER MANAGEMENT SYSTEM IN A COMPUTING DEVICE		
Application No.:	09/876,291	Filed:	June 7, 2001
Examiner:	Mark A. Connolly	Group Art Unit:	2115
Atty. Docket No.:	1001-0179	Confirmation No.:	9539

February 26, 2007

Mail Stop Appeal Briefs - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed on December 26, 2006. The fee required under 37 C.F.R. § 41.20(b)(2) is being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 41.20(b)(2), § 1.16, or §1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 50-0631.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., the assignee of record, as evidenced by the assignment recorded at Reel/Frame 011908/0016.

RELATED APPEALS AND INTERFERENCES

Known prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal include:

None.

STATUS OF CLAIMS

Claims 1-9, 19, and 20-22 are pending. Claims 10-18, 20, and 23-32 have been canceled. Claims 1-9, 19, and 20-22 stand rejected and are the subject of this appeal.

STATUS OF AMENDMENTS

Amendments to claims 1, 16, and 24 were filed November 14, 2006 in response to the final Office action. The Advisory Action mailed December 6, 2006 indicates those amendments were entered for purposes of appeal. An amendment was filed under 37 C.F.R. § 41.33(a) on February 21, 2007 to correct an informality in claim 2. In addition, an amendment was filed under 37 C.F.R. § 41.33(a) on February 22, 2007 canceling claims 10, 14-18, 23, 24, and 26-28. It is presumed both amendments will be entered for purposes of this appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to managing power consumption in a computing system having several possible processing performance states. If the power management control function determines that additional performance is necessary to meet performance requirements based on utilization of the integrated circuit, rather than increasing the performance state one step at a time, the power management control function selects the maximum performance state (or near maximum) regardless of the current performance state. See page 7, lines 12-18. Fig. 3 illustrates that concept. Assume the processor has five performance states P1-P5, with P5 being the highest and P1 the lowest. Whenever the power management determines that a higher performance state is required when operating at any of the levels P1-P4, power management selects the maximum performance state P5 as the next performance state. Thus, if the performance state is always taken straight to the maximum performance state when a performance increase is required, rather than stepping up to the maximum performance state through the other performance states, there is less of a chance that a user would notice any performance degradation. See page 7, line 30 to page 8, line 4. That is especially true when the task that needs the increased performance requires a near real-time response, for instance, while decoding an audio or video file. See

page 7, lines 23-25. In effect, the power management control function anticipates a peak loading by assuming that any indication of a required increase in performance is assumed to be a burst requiring peak performance. See page 8, lines 1-4. Fig. 5 illustrates an exemplary embodiment of a processor that can dynamically adjust its operating parameters to provide power management in accordance with processor utilization. See page 17, line 22 – page 19, line 22 for a description of how performance adjustment may be accomplished in the embodiment illustrated in Fig. 5.

Claim 19 includes means for determining utilization of the integrated circuit. Means for determining utilization may be provided by software as described, e.g., on page 9, line 29, to page 10, line 6. In a preferred embodiment, the power management control function is provided by power management software, which periodically extracts the utilization information by querying the operating system (OS). See page 7, lines 20-22. In one embodiment, the power management software queries the operating system periodically for an enumeration of the tasks that are running on the operating system. In addition, the power management software obtains execution statistics for each of the enumerated tasks, including those tasks that are part of the operating system, in order to determine how much CPU time the various tasks have used. The power management software then uses that information to create an overall utilization index for comparison to the high and low thresholds. In addition to the amount of CPU time used by a task, each task also has a priority, which may also be utilized by the power management software in determining the utilization index as described further herein. See page 9, line 23 to page 10, line 6. Fig. 4 shows exemplary statistics that can be obtained for the utilization determination. Additional details on various aspects of obtaining utilization information can be found on page 10, lines 7, to page 14 line 2. Such additional details include the ability to average utilization information to allow the system to react more slowly to changes, frequency of task enumeration, excluding certain tasks from the utilization calculation (e.g., low priority tasks), or ignoring kernel time. As explained on page 14, lines 3-12, the power control software in one embodiment is a driver running under the operating system. In a preferred embodiment, the software to implement the driver is actually in two parts. A part resides at an application level. That part queries the OS for information on CPU utilization by the various tasks running under the OS. Software at the application level also performs the sample averaging, compares the samples to the high and low threshold levels and determines if a performance change is required.

A second part of the power control software operates at a high privilege level (e.g., ring 0) and interacts directly with BIOS tables and hardware registers to determine actual run states in terms of voltage/frequency values.

Claim 19 also includes means for changing, while in each of the performance states other than a maximum performance state, from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization. The description of the functioning of this element is illustrated in Fig. 3, described above, and described on page 7, line 12, to page 8, line 4. In addition, exemplary structure for effectuating a change in performance state is illustrated in the processor in Fig. 5 and the associated description, and the software necessary to change the operating parameters such as voltage and frequency to effect the change in performance state is described. The process to effectuate the change is illustrated in Fig. 6 and described on page 19, lines 23-28.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I: The rejection of claims 1-2, 4-5, 8-19, 21-24, and 26-28 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,954,820 to Hetzler.

Ground II: The rejection of claim 3 under 35 U.S.C. § 103(a) as obvious over U.S. Pat. No. 5,954,820 to Hetzler.

Ground III: The rejection of claims 6 and 7 under 35 U.S.C. § 103(a) as obvious over Hetzler in view of U.S. Pat. No. 5,787,294 (Evoy).

ARGUMENT

Ground I: The rejection of claims 1-2, 4-5, 8-19, 21-24, and 26-28 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,954,820 to Hetzler.

Under 35 U.S.C. § 102(b), each element of a claim must be found in the single prior art reference, either expressly or inherently. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson

Orthopaedics, Inc., 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). If the reference fails to teach even one limitation of a claim, then the claim is not anticipated. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir.1986). See Akzo N.V. v. U.S. Int'l Trade Comm'n, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986) ("Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in a prior art reference.")

Claims 1-9

With respect to claim 1, applicants respectfully traverse the rejection of claim 1 as anticipated by Hetzler. Hetzler is directed to a method for managing power in a portable computer using past access history and a prediction of future user demands. See Abstract. The majority of Hetzler's teaching is directed to optical storage devices, but Hetlzer states the invention is equally applicable to any component of the mobile computer. See page 25, lines 6-10. Thus, for a CD-ROM drive Hetzler teaches there are various power modes SEEK/READ, IDLE, IDL2, and STANDBY. See Table 2 in col. 7.

The preamble of claim 1 recites *a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit* as explained below. The preamble of claim 1 should be considered to limit the claim because the definition of the performance states is important to properly interpret the claims. "A preamble limits the [claimed] invention if it recites essential structure or steps, or if it is `necessary to give life, meaning, and vitality' to the claim." Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002). That is, "when the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615 (C.A.Fed. (N.J.), 1995) In re Paulsen, 30 F.3d 1475, 1479, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994)("[T]erms appearing in a preamble may be deemed limitations of a claim when they give meaning to the claim and properly define the invention.") [internal quotation omitted]. Thus, the proper interpretation of performance states in claim 1 requires the performance states that are referred to in the body of the claim be construed as *a plurality of performance states,*

including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit.

Claim 1 further requires determining utilization of the integrated circuit. The Office action apparently relies on controller 56 as corresponding to the claimed integrated circuit. ("Hetzler teaches that utilization of controller 56 is dependent upon ... access of the CD-ROM drive itself.") The Office action further relies on Fig. 8 and col. 6, lines 41-64. Fig. 8 shows three power levels: the SEEK/READ power P0, the IDLE power P1, and the power mode P2. Accesses at P0 consume the most power, P1 intermediate power and P2 the least power. It is also noted the IDLE power mode is the normal track-following operation when data is not being read and no seek is occurring. Hetzler uses the term "active state" to refer to the drive when it is in either the SEEK/READ or the IDLE modes. Hetzler also teaches that additional energy is consumed during read operations because more portions of controller electronics 56 are active. Hetzler, at col. 6, lines 30-32.

Hetzler teaches two common power-save modes referred to as IDLE2 and STANDBY. Hetzler, at col. 6, lines 32-55. In the IDLE2 mode, actuator 63 is parked and servo control electronics 53 and read electronics, including pre-amplifier and channel 54, are turned off to reduce power usage. In the STANDBY mode, the actuator 63 is moved to its parking location, and spindle motor 62 and spindle drive 51 are turned off. The STANDBY mode purportedly has all of the power savings of the IDLE2 mode, plus the additional reduction in power to spindle control electronics portion of controller 56 and spindle drive 51. Thus, applicants agree that Hetzler teaches that different power is consumed by controller 56 in various power modes.

Claim 1 further requires that each time the computing system determines that a higher performance state is required based on the determined utilization while in each of the other performance states, changing to a predetermined performance state, skipping all intermediate performance states between a current performance state and the predetermined performance state.

The final Office action relies on Fig. 8 showing P1 and P2 going to the P0 state as teaching that Hetzler teaches always going to a predetermined state as claimed. First, there is no teaching in Hetzler that the active power modes SEEK/READ and IDLE (see col. 6, lines 32-35)

have different performance capabilities. The claim requires *a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit.* In fact, applicants submit that it is reasonable to assume that the capabilities in the two active power modes SEEK/READ and IDLE are identical. While the operations being performed in P0 and P1 are different and thus the power consumption is different, the capabilities of the circuitry are identical (e.g., same voltage and same frequency). In contrast, applicants claim different performance capabilities for the claimed performance states (e.g., through different clock speeds and/or voltage levels – see claims 6, 7). The final Office action states that "it should be apparent that when the CD-ROM drive jumps to the high power P0 state from either the lower power P1 or P2 state (as seen in Fig. 8), the power/performance mode of the controller 56 would change accordingly." However, Hetzler does not teach different capabilities for P0 and P1 as explicitly required by the claim. Thus, with reference to Fig. 8 of Hetzler, while there is different power consumption between P0, P1, and P2, there is no teaching that the controller 56 has different performance capabilities in P0 and P1 as required by claim 1.

The Advisory Action points out correctly that Hetzler teaches additional power savings states such as STANDBY and SLEEP. However, Hetzler does not teach with respect to the CD controller that it always comes out of STANDBY and SLEEP and goes to PO or to P1. Hetzler teaches only going to the active state (as also pointed out in the Advisory), which is either P0 or P1. See col. 15, lines 30-38. It is entirely conceivable that Hetzler comes out of the sleep state to the IDLE state. Hetzler is silent on the matter.

Other parts of Hetzler fail to make up for the deficiencies of Fig. 8. Hetzler teaches with respect to Fig. 5 in 306 that if "freq <= tf[mode], then the performance mode is entered in 310. Hetzler tests in the order of the most energy savings to the least energy savings to save the most energy. Col. 12, lines 60-65. If the mode is not entered after 306, it is decremented by one in 309 to a mode that has less energy savings, i.e., more power consumption. That way the power consumption mode is stepped up or down based on the threshold, as explained in col. 12, lines 39-59. If the access frequency (freq) is greater than the threshold frequency, then the mode is not entered. Applicants further note that Hetzler further teaches in Fig. 5 that the power mode may be gradually increased (to greater performance) at step 309. In Fig. 5, the maxmode is the biggest power savings mode, so (mode-1) provides less power savings corresponding to more

performance. Thus, Hetzler in Fig. 5 teaches away from the claimed invention of always going to the predetermined performance state (generally the maximum performance mode – as recited in claim 2) if integrated circuit utilization indicates that a higher performance state is required.

Thus, applicants maintain that Hetzler fails to teach always going to the predetermined (or maximum) performance state as recited in claim 1 (or claim 2).

With respect to Fig. 8, Hetzler also fails to teach that the change between the active states P1 and P0 is *based on the determined utilization of the integrated circuit* as required by claim 1 (i.e., of what the Office action deems corresponds to the claimed integrated circuit – namely controller 56). Instead, the movement from P1 to P0 seems to be based solely on an access request. Thus, Fig. 8 of Hetzler does not teach each time the computing system determines that a higher performance state is required based on the determined utilization while in each of the other performance states, changing to a predetermined performance state, skipping all intermediate performance states between a current performance state and the predetermined performance state.

In the Advisory action the Examiner argues that a periodic access pattern and actual component access are interpreted as utilization. Applicants respectfully disagree. The claim requires changing, based on a determined utilization while in each of the other performance states, to the predetermined performance state. An actual access request, shown in Fig. 8 of Hetzler is not a determined utilization, it is a request for utilization. Further, the periodic utilization (access patterns) is not determined *while in each of the other performance states*, it is necessarily utilization determined during the active state. See col. 24, lines 21-44. Hetzler teaches at col. 15, lines 30-38 that:

> Once a power save mode has been entered, it may be exited either by entering another power save mode or by returning the component to the active state. The former occurs when the estimated access frequency continues to drop, crossing the threshold frequencies of other modes. The latter occurs when either a component access occurs or when a periodic access pattern has been detected."

In the instant invention, utilization is determined in the current integrated circuit (e.g., processor state) based on, e.g., processor utilization. If the performance capability of the processor is too low because voltage and/or frequency are too low, they are increased to increase

performance. In contrast, Hetzler simply responds to an actual access request and or an expected access. Since Hetzler teaches entering the active state in response to a component access or a periodic access pattern, which is not determining *that a higher performance state is required based on the determined utilization while in each of the other performance states,* applicants submit Hetzler does not teach this aspect of claim 1.

Thus, because Hetzler does not teach one or more elements of claim 1, expressly or inherently, applicants submit that claim 1 and all claims dependent thereon, distinguish over Hetzler. Accordingly, the Board is respectfully requested to reverse the rejection of claims 1-9.

Claim 9

Claim 9 recites that the integrated circuit includes a central processing unit. Clearly, controller 56 does not include a central processing unit. However, Hetzler contemplates application of the invention to CPU 4 in col. 25. Claim 1 requires *a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit.* Hetzler teaches at col. 25, lines 30-34, that all components have at least two modes of operation, an ACTIVE mode, which is typically full operational mode, and at least one less than full operation or reduced power mode, which is typically the OFF mode.

At col. 25, lines 34-37, Hetzler teaches that many devices have more modes, such as a reduced clock rate mode for the CPU 4. Hetzler does not specifically teach that the CPU goes from the reduced clock rate mode and the OFF mode to the full operational mode. However, it is reasonable to assume that CPU 4 would go to the full operational mode both from the OFF mode in response to a power on and to the full operational mode from the reduced clock rate mode. However, claim1 requires the computing system determine that a higher performance state is required based on the determined utilization while in each of the other performance states. There is no determined utilization for the CPU while it is OFF. Nor are the IDLE/SEEK and standby modes described in association with the CD controller applicable to CPU4. Thus, with respect to the CPU 4, Hetzler fails to teach the combination of the elements of claims 1 and 9.

Accordingly, the Board is respectfully requested to reverse the rejection of claim 9 for this additional reason.

Claims 19, 21, 22

With respect to claim 19, applicants respectfully submit, as pointed out above with respect to Fig. 8, that Hetzler also fails to teach the "means for changing." Specifically, applicants submit that Hetzler fails to teach *while in each of the performance states other than a maximum performance state, changing from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.* The Office action relies on the change between the active states P1, and P0 is based on utilization of the integrated circuit (what the Office action deems corresponds to the claimed integrated circuit – i.e., controller 56). However, the change between the active states is not based on the determined utilization of the integrated circuit as recited in claim 19, but upon an access. See col. 18, lines 32-49. Thus, Hetzler fails to teach *while in each of the performance states other than a maximum performance state, changing from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.* Accordingly, applicants respectfully submit that claim 19 and all claims dependent thereon distinguish over the references of record and respectfully request the Board reverse the rejection of those claims.

Ground II: The rejection of claim 3 under 35 U.S.C. § 103(a) as obvious over U.S. Pat. No. 5,954,820 to Hetzler.

In rejecting claim 3, the Office action fails to establish a *prima facie* case of obviousness because Hetzler fails to teach or suggest the claimed combination. See In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987); see also In re Kahn, 441 F.3d 977, 986, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006). In general, obviousness is a legal determination based on underlying factual inquiries. See Minnesota Min. & Mfg. Co. v. Johnson & Johnson

Orthopaedics, Inc., 976 F.2d 1559, 1572-73, 24 USPQ2d 1321, 1332-33 (Fed. Cir. 1992). Graham v. John Deere Co., 383 U.S. 1, 17 (1966) defines the factual inquiries utilized to evaluate the prior art. Specifically, the prior art is evaluated in terms of: (1) its scope and content; (2) the differences between the prior art and the claimed invention; (3) the level of ordinary skill in the art at the time the application was filed; and (4) objective, or secondary, evidence of nonobviousness such as commercial success, failure of others, long-felt need and unexpected results, which must be considered in reaching a conclusion of obviousness. See Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 460 (1966); Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1566-67, 1 USPQ2d 1593, 1595-96 (Fed. Cir. 1987); Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1573, 24 USPQ2d (BNA) 1321, 1333 (Fed. Cir. 1992).

In the present appeal, the issue relates the position taken in the Office action that "applicant's numerous predetermined performance states are construed to be an admission that the criticality does not reside in which performance state is entered and thus obvious variations of one another." Applicants have made no such admission. The applicants respectfully submit that Hetzler fails to teach or suggest that the predetermined performance state is a near maximum performance state as claimed. As the Office action has not provided any reference or other basis to modify Hetzler to achieve claim 3, applicants respectfully submit that a prima facie case of obviousness has not been established. Further, applicants note that for the reasons described above with relation to claim 1, Hetzler fails to teach those elements of claim 1 identified above from which claim 3 depends. Therefore the Board is respectfully requested to reverse the rejection of claim 3 as obvious over Hetzler.

Ground III: The rejection of claims 6 and 7 under 35 U.S.C. § 103(a) as obvious over Hetzler in view of U.S. Pat. No. 5,787,294 (Evoy).

Claims 6 and 7

In rejecting claims 6 and 7, applicants submit that the Office action fails to establish a *prima facie* case of obviousness because Hetzler, alone or in combination with Evoy, fails to teach or suggest the claimed combination in either claim. See In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987); see also In re Kahn, 441 F.3d 977, 986,

78 USPQ2d 1329, 1335 (Fed. Cir. 2006). Specifically, for the reasons described above with relation to claim 1, Hetzler fails to teach those elements of claim 1 identified above from which claims 6 and 7 depend. Evoy fails to make up for those deficiencies. Therefore, the Board is respectfully requested to reverse the rejection of claims 6 and 7 as obvious over Hetzler in view of Evoy.

CONCLUSION

For at least the foregoing reasons, appellants respectfully submit that claims 1-9 and 19, and 21-22 distinguish over Hetzler, alone or in combination with Evoy. Accordingly, the Board is respectfully requested to reverse the rejections of claims 1-9, 19, and 21-22 and to direct the claims of the present application to be issued.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

- ☐ deposited with the US Postal Service with sufficient postage as first class mail in an envelope addressed as shown above.
- ☐ facsimile transmitted to the USPTO.
- ☒ transmitted using the USPTO electronic filing system.

Mark Zagorin — 2/26/07
Mark Zagorin — Date

EXPRESS MAIL LABEL: _____

Respectfully submitted,

Mark Zagorin

Mark Zagorin, Reg. No. 36,067
Attorney for Applicant(s)
(512) 338-6311
(512) 338-6301 (fax)

CLAIMS APPENDIX

1. A method of managing power consumption in a computing system having a plurality of performance states, including a maximum performance state and a plurality of other performance states that provide successively less performance capability for an integrated circuit, the method comprising:

determining utilization of the integrated circuit; and

each time the computing system determines that a higher performance state is required based on the determined utilization while in each of the other performance states, changing to a predetermined performance state, skipping all intermediate performance states between a current performance state and the predetermined performance state.

2. The method as recited in claim 1 wherein the predetermined performance state is a maximum performance state.

3. The method as recited in claim 1 wherein the predetermined performance state is a near maximum performance state.

4. The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value; and

if the integrated circuit utilization is below the second threshold utilization value, always entering a next lower performance state as a next performance state.

5. The method as recited in claim 1 further comprising:

comparing the determined utilization to a threshold utilization value to determine if a higher performance state is required;

comparing the integrated circuit utilization to a second threshold utilization value;

if the integrated circuit utilization is below the second threshold utilization value,

entering a lower performance state as a next performance state, the lower performance state being determined according to integrated circuit utilization.

6. The method as recited in claim 4 wherein the performance state is lowered by reducing at least one of the voltage and frequency.

7. The method as recited in claim 1 wherein the performance state is reduced by reducing both voltage and clock frequency of the integrated circuit.

8. The method as recited in claim 1 wherein determining the utilization is done periodically.

9. The method as recited in claim 1 wherein the integrated circuit includes a central processing unit.

10. - 18. (Canceled)

19. A computing system comprising:

an integrated circuit having multiple performance states;

means for determining utilization of the integrated circuit; and

means for changing, while in each of the performance states other than a maximum performance state, from a current performance state to the maximum performance state, skipping all intermediate performance states between the current performance state and the maximum performance state, each time the computing system determines that a higher performance is required based on the determined utilization.

20. (Canceled)

21. The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for always changing operation of the integrated circuit from the current performance state to a next lowest performance state in response to a determination that the utilization is below a second threshold utilization value.

22. The computing system as recited in claim 19 further comprising:

means for determining that the utilization is below a second threshold value and for changing operation of the integrated circuit from the current performance state to a lower performance state in response to a determination that the utilization is below a second threshold utilization value, the lower performance state being determined according to the integrated circuit utilization.

23. - 32 (Canceled)

EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.